sPHENIX silicon tracker: concept and the status of sensor R&D

May 12, 2015

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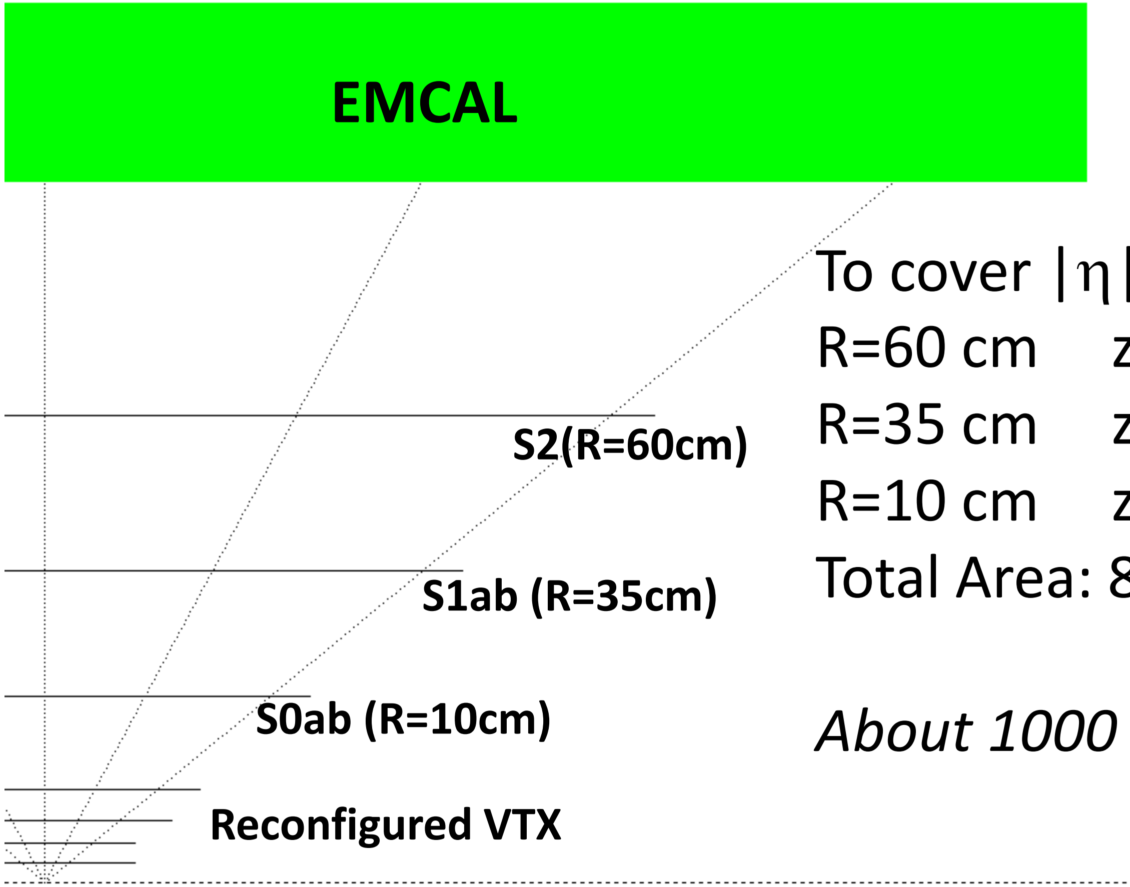
Tracker concept



To cover $|\eta|<1.1$

R=60 cm zmax = 80cm Area = $6.0m^2$

R=35 cm zmax = 45cm Area = $2.0m^2$

R=10 cm zmax = 14cm Area = $0.2m^2$

Total Area: 8.2 m^2 of silicon (single layer)

About 1000 10x10cm sensors needed

This configuration is somewhat smaller than the version in MIE update.
This configuration should achieve upsilon mass resolution of 100MeV if the radiation thickness of the middle layer (S1ab) is 1.5% X0.
As I will show later, 1.5% radiation length is feasible to achieve
In MIE, it is assumed to be 2%. → Outer radius need to be expaned to ~80cm

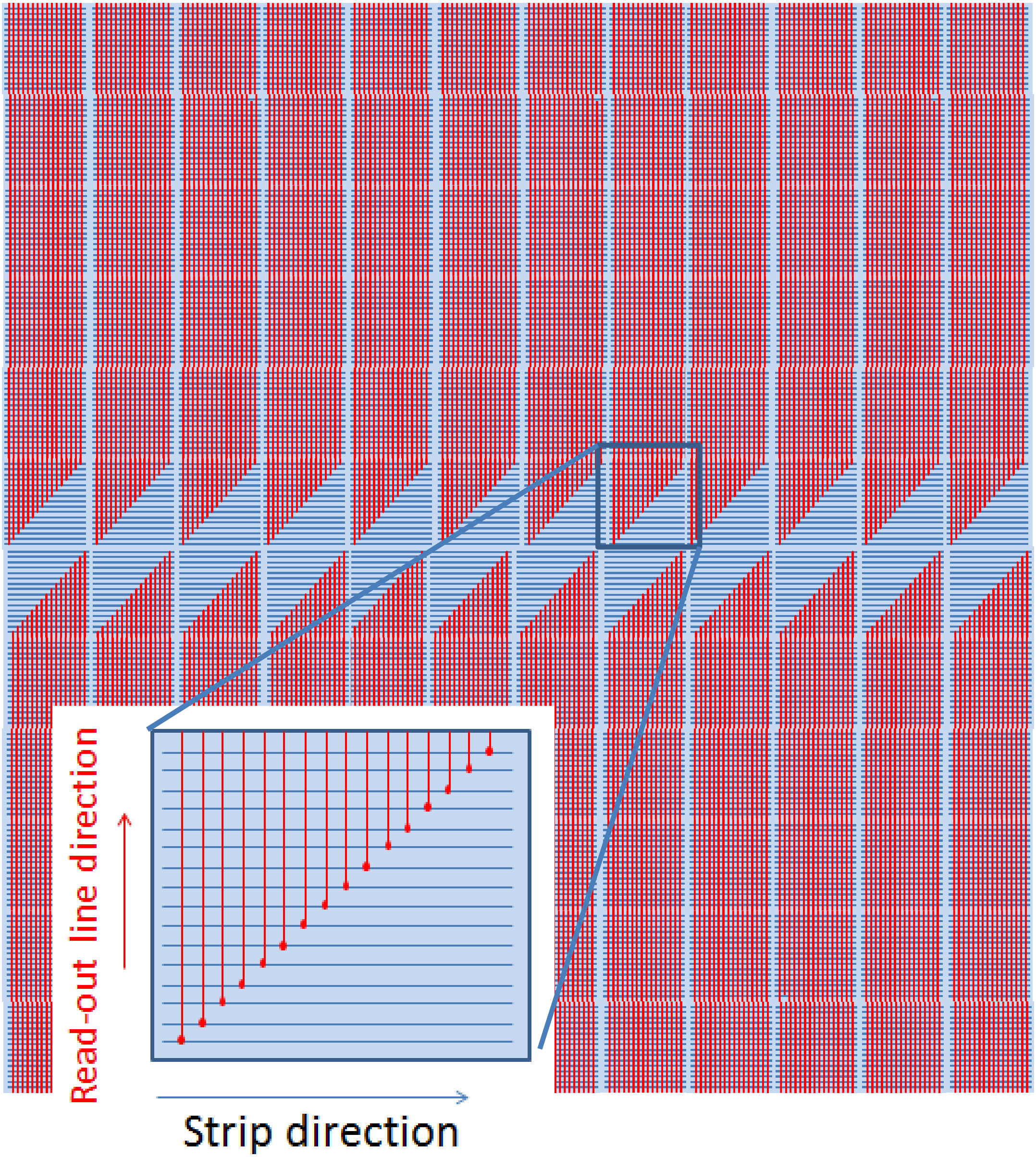
Tracker concept

Layer	R (cm)	SM/ladder	# of ladder	# of SM	SVX4/SM	# of SVX4
S0ab	10	3	40	240	12	2880
S1ab	35	8	42	672	24	16128
S2	60	14	40	560	24	13440

- 3 types of sensor

10 cm x 10 cm	for S2	no stereo
10 cm x 5 cm	for S1	stereo
10 cm x 1.6 cm	for S0	stereo

Concept of S2 sensor

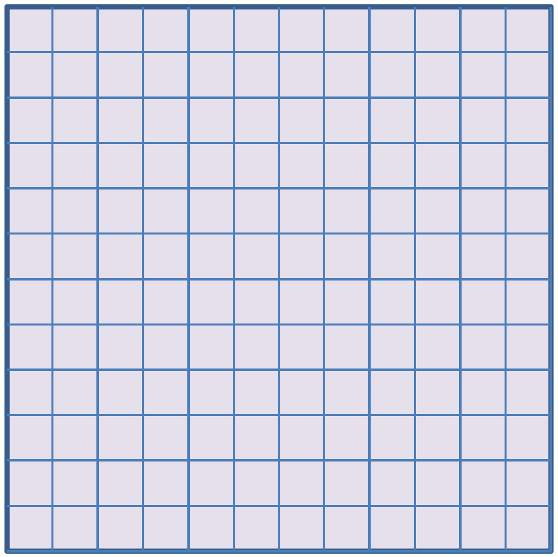


- 96mmx92.16mm active area
- Divided into 12x12 blocks
- Each block is 8mm x 7.68mm and made of 128 strips of 8mm x 60 micron
- Upper 6 bocks are connected upwards.
- Lower 6 blocks are connected by downwards
- 24 SVX4 chips to read-out the entire sensor

3 sensors

S2 sensor

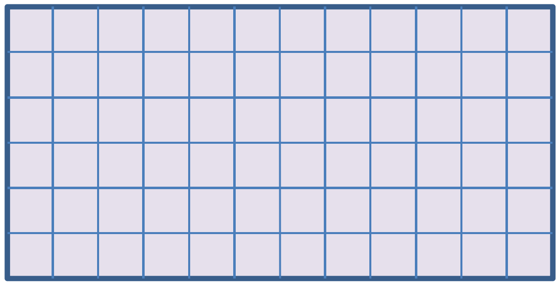
Bonding pads for 12 SVX4s



Bonding pads for 12 SVX4s

S1 sensor

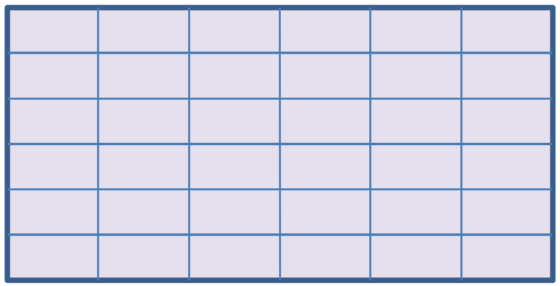
Bonding pads for 12 SVX4s



Bonding pads for 12 SVX4s

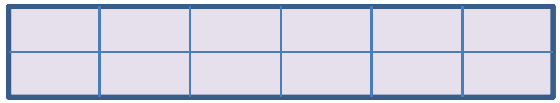
OR

Bonding pads for 12 SVX4s

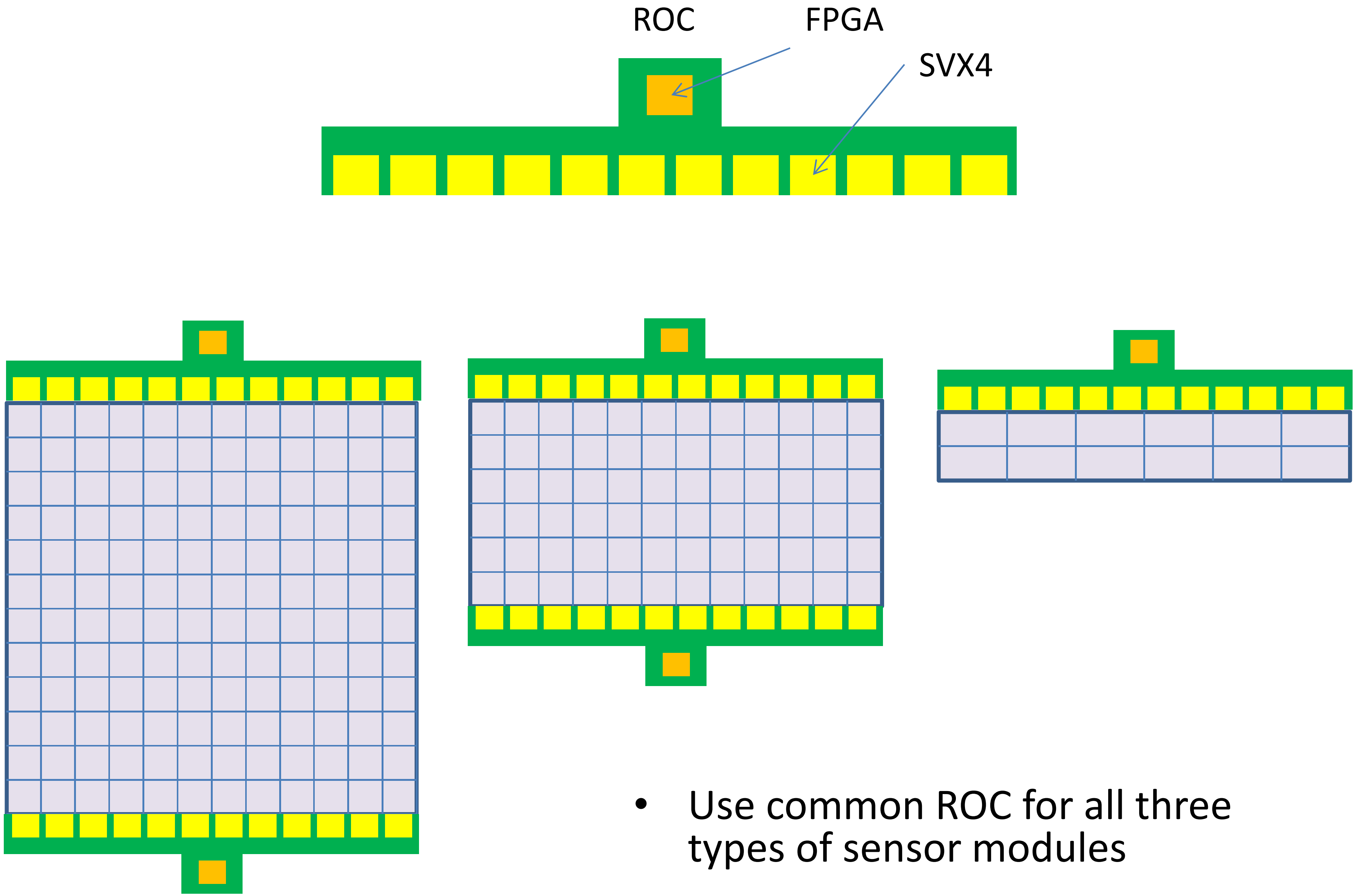


S0 sensor

Bonding pads for 12 SVX4s

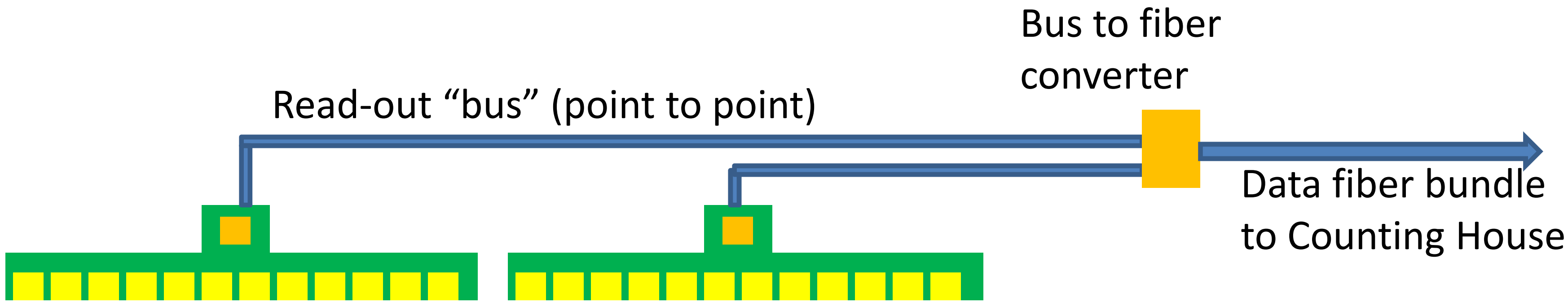


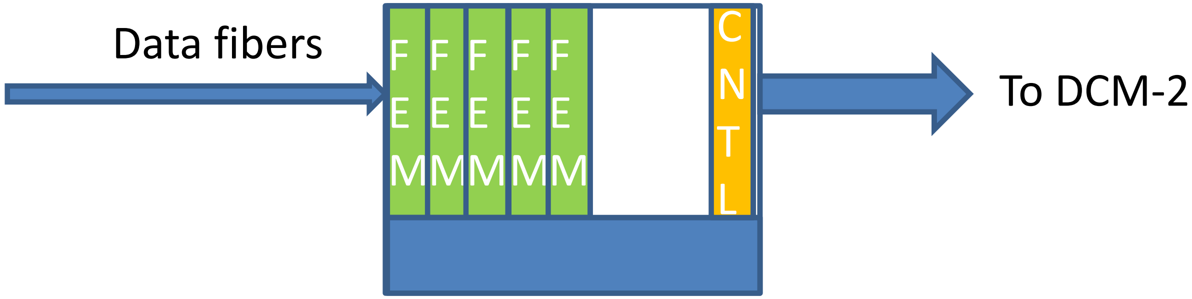
ROC and sensor modules



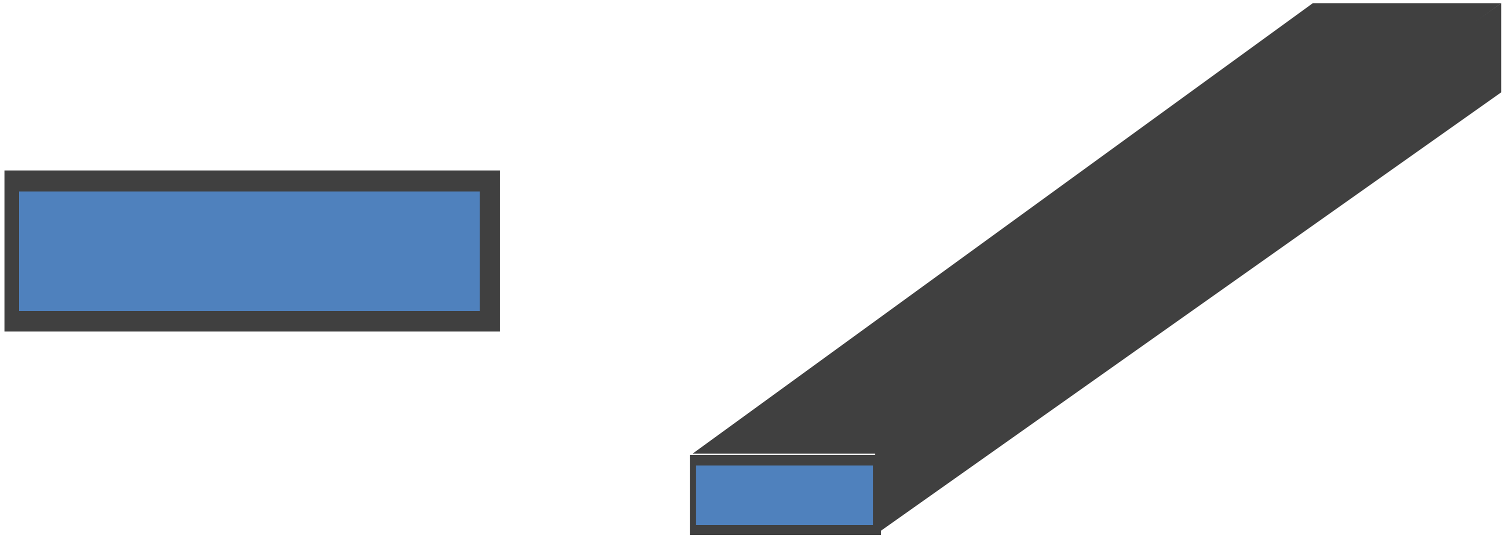
- Use common ROC for all three types of sensor modules

Read-out scheme (Final)



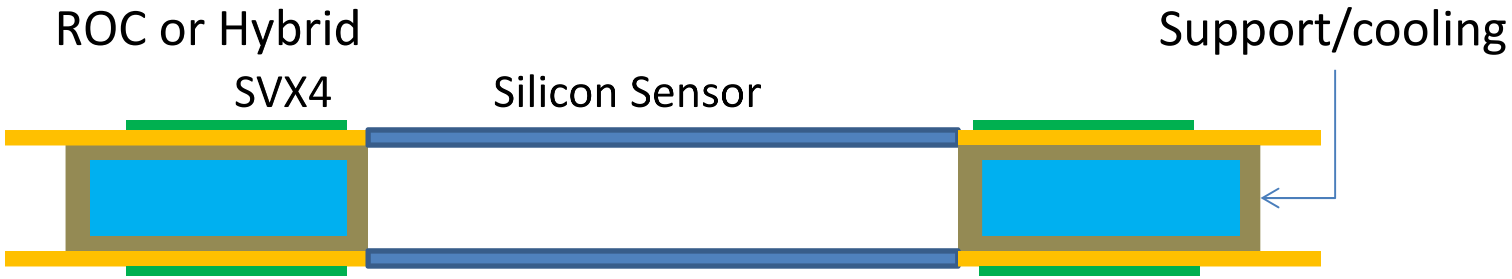


Stave prototype

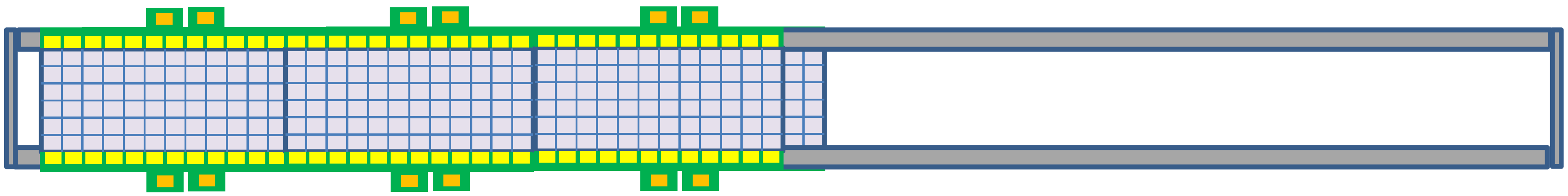


- Rectangular channel for cooling and support
- Make a few to cool ROC and to operate it.

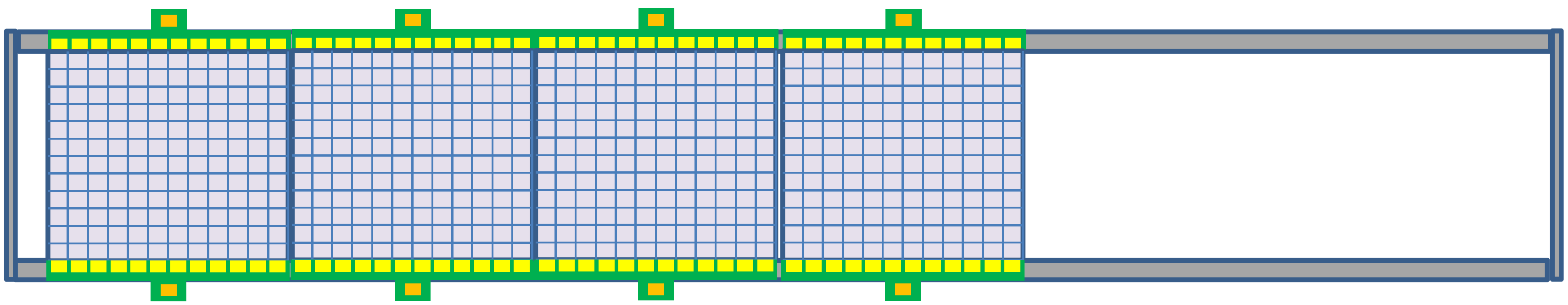
Prototype ladder



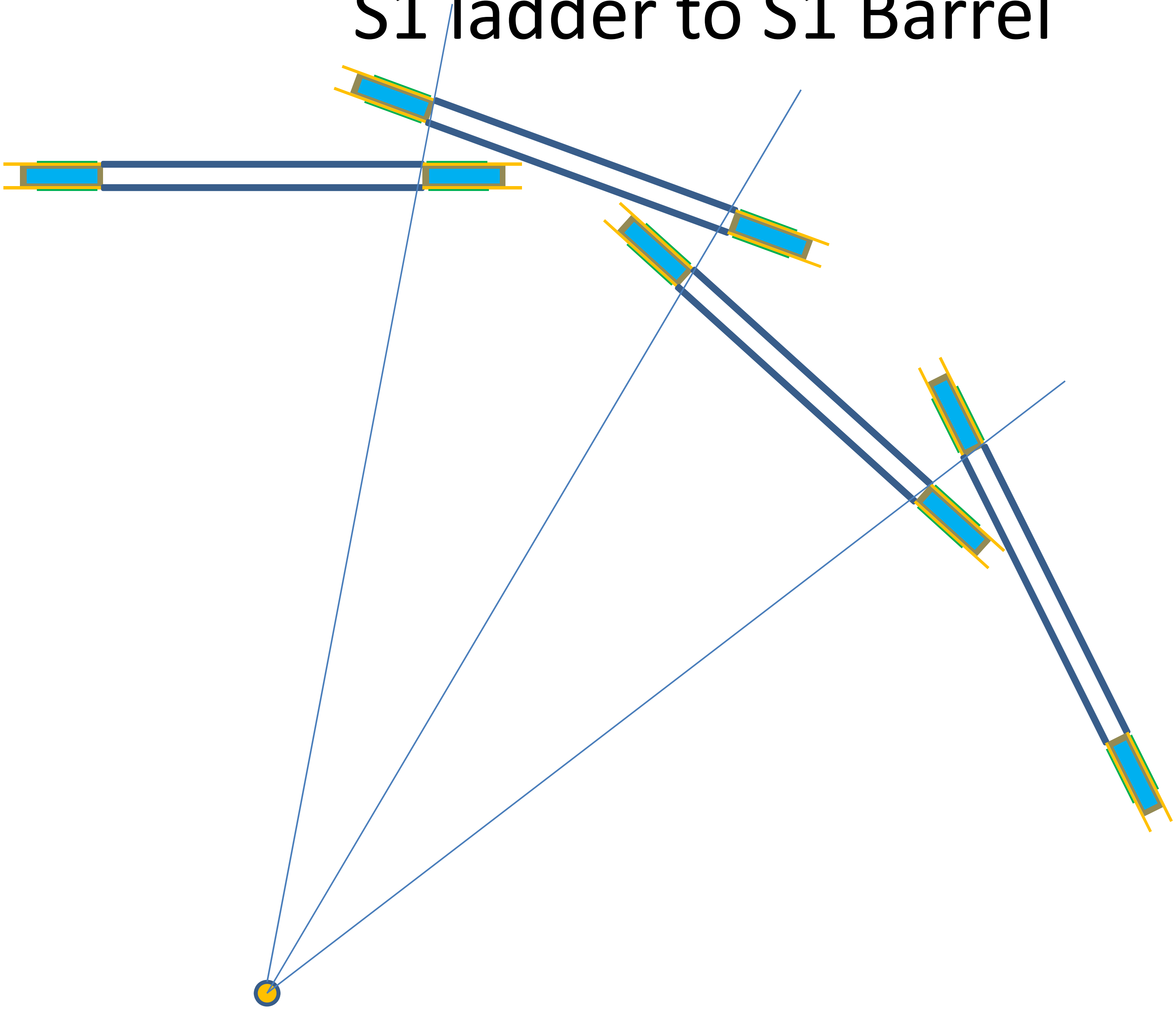
S1a/b ladder (double layer)

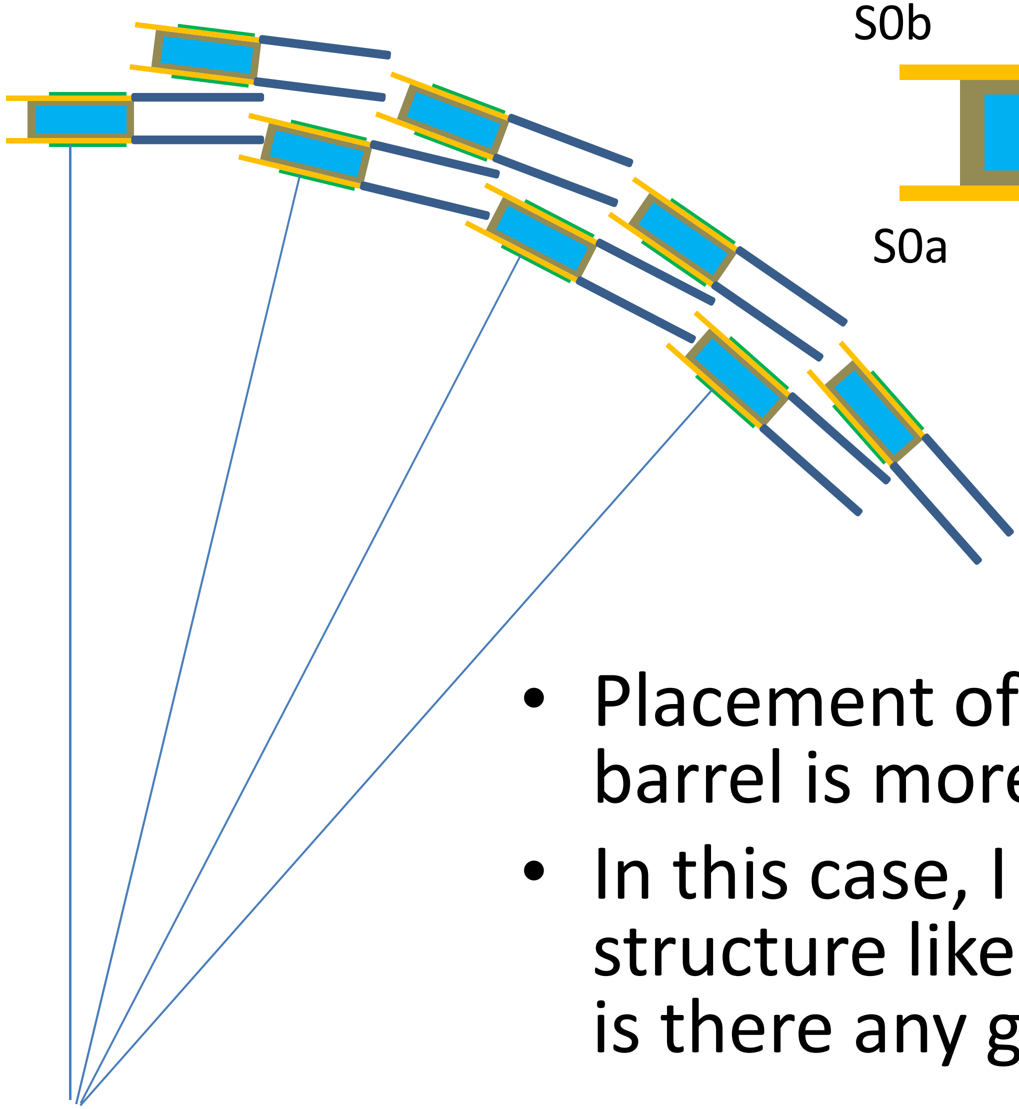


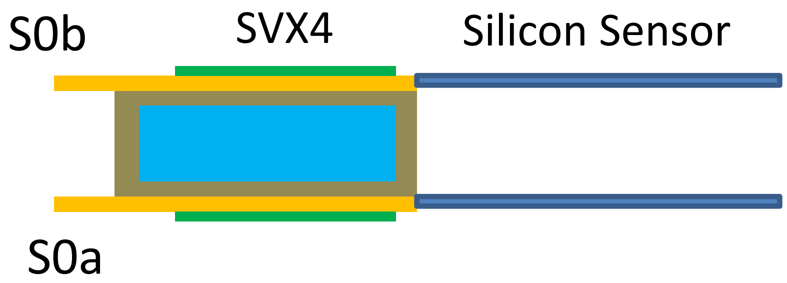
S2 ladder (single layer)



S1 ladder to S1 Barrel

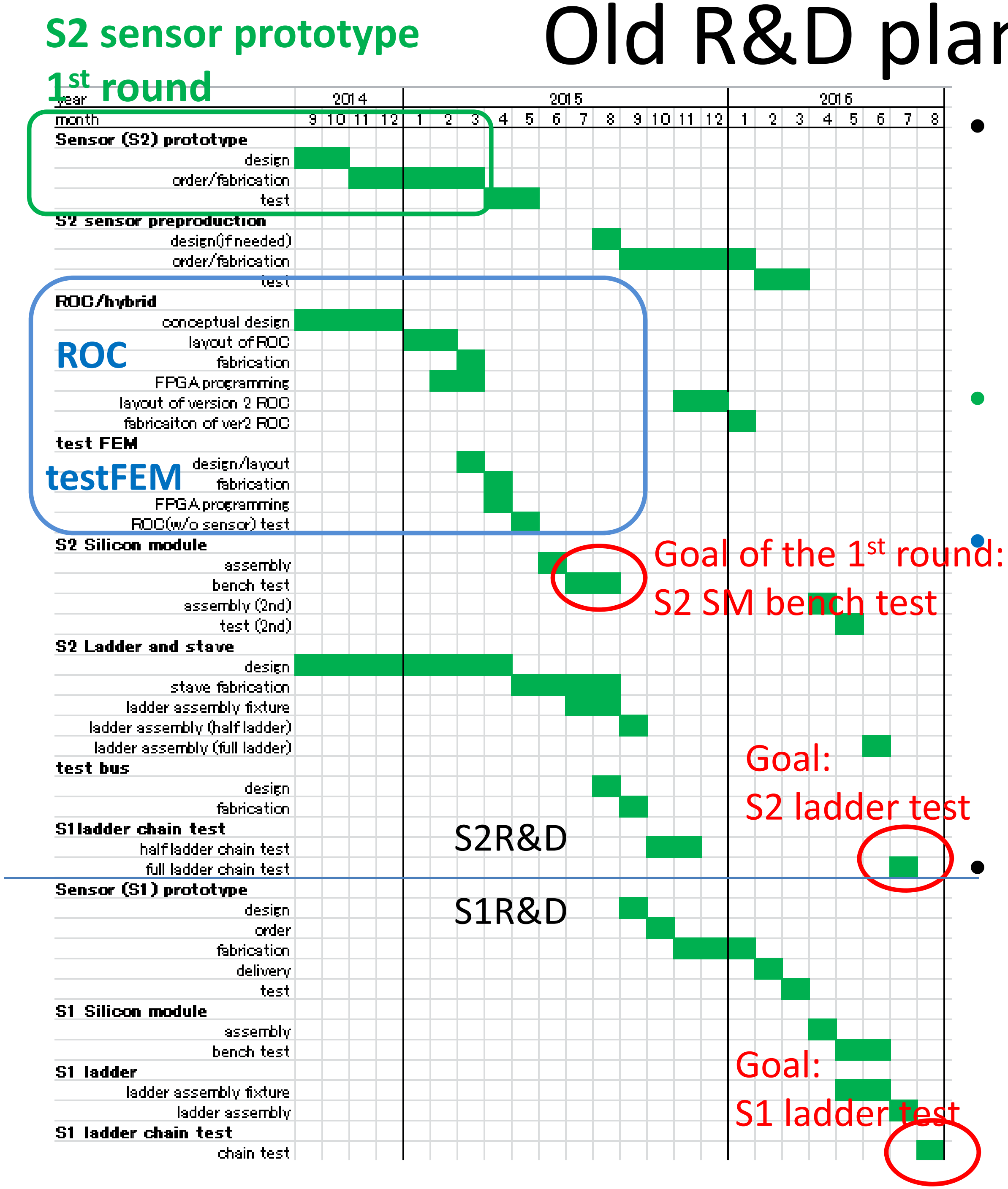






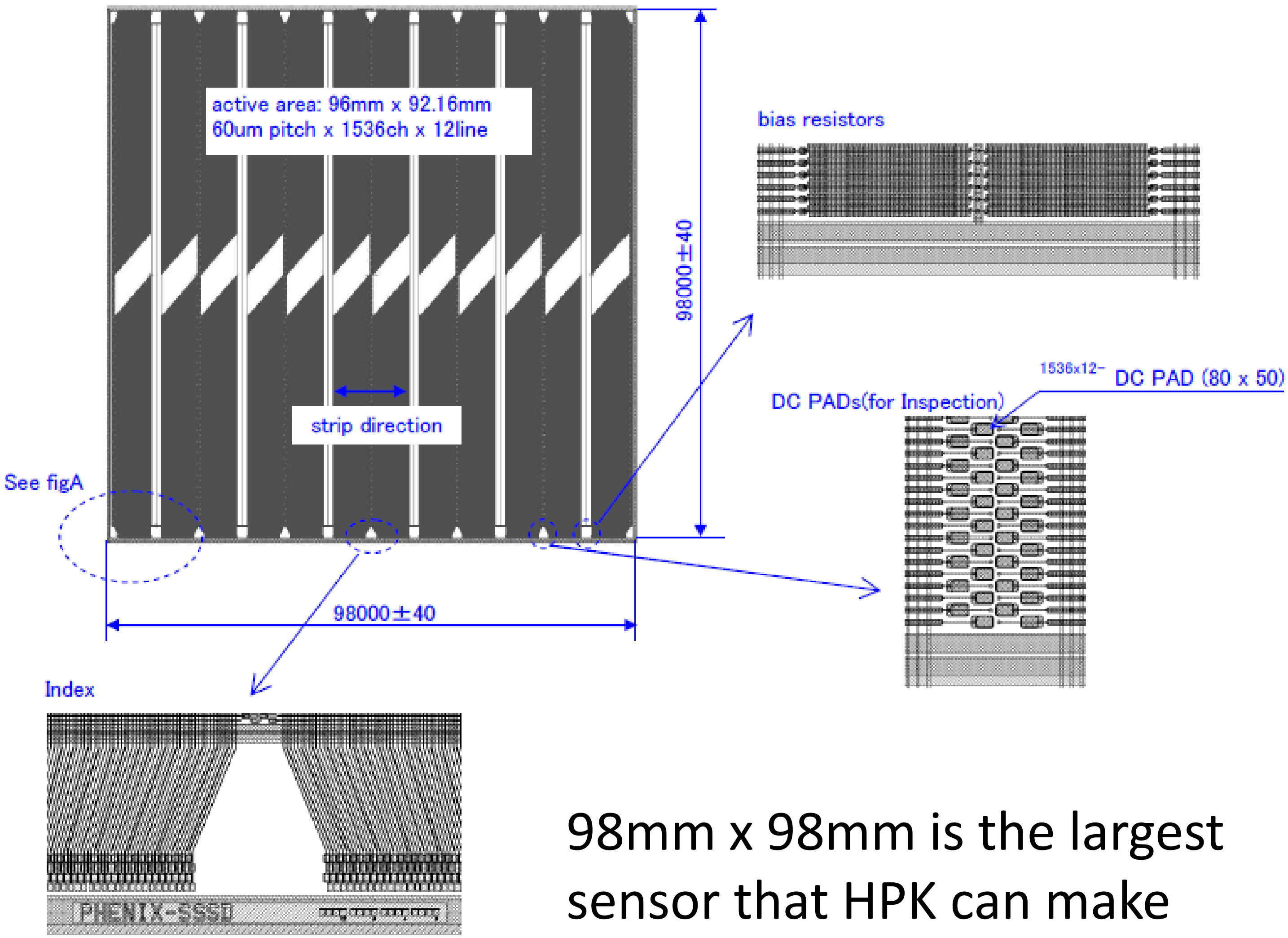
- Placement of S0 ladder into a barrel is more challenging
- In this case, I think one-sided structure like above is needed. (or is there any good idea?)

Old R&D plan



- This is an R&D plan that I made in August 2014 in the context of sPHENIX R&D request
- Good news: 5 S2 sensors were delivered
- Bad news: No progress in the next part: ROC and FEM development
  - Without ROC and FEM, we cannot test the sensor
- Need engineering support to make progress

HPK design for the S2 sensor



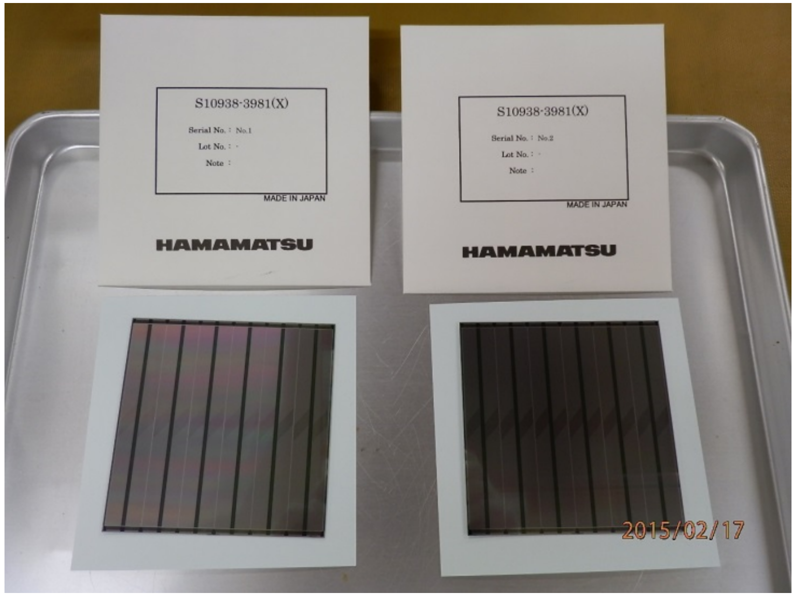
98mm x 98mm is the largest sensor that HPK can make

Pad pattern is the same as the stripxel sensor and matches the input pad pattern of SVX4

S2 sensor protoye

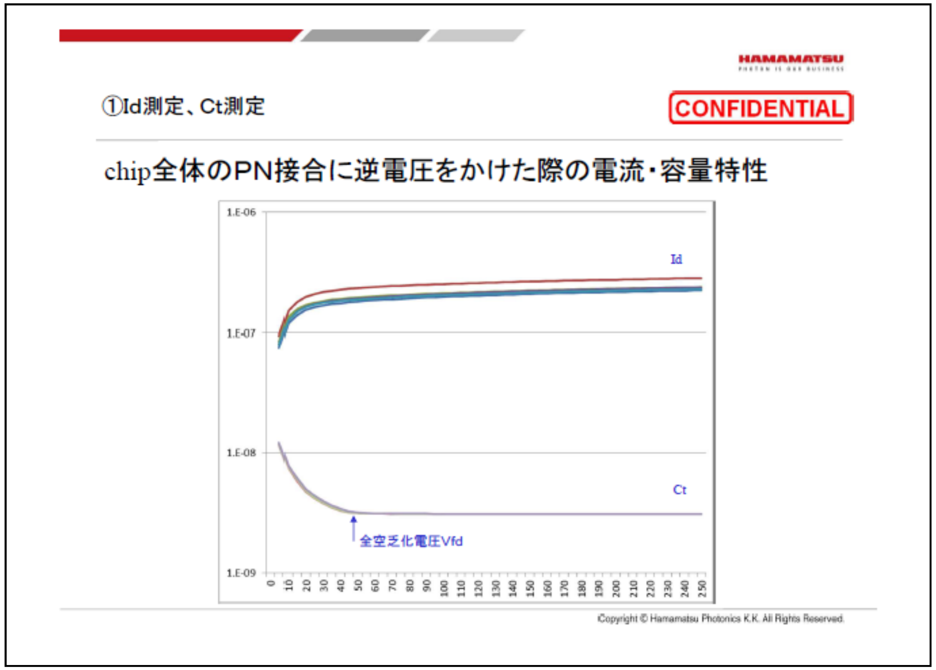
- We (RIKEN and JAEA) ordered S2 sensor prototype to HPK
  - Ordered 5 sensors
    - (mask, set up, etc)+3 sensors : RIKEN
    - 2 additional sensors: JAEA
  - They will be tested at HPK and 5 good sensors that satisfies the specification will be delivered.
- The contract was made on November 21.
- 2 JAEA sensors were delivered on Feb 16, 2015
  - They are Tested by HPK, and 2 good sensors are delivered
  - Susumu Sato (JAEA) went to HPK to inspect the sensor
- 3 RIKEN sensors delivered to RIKEN in March 2015
- Total of 5 sensors are now in RIKEN

Prototype sPHENIX silicon sensor

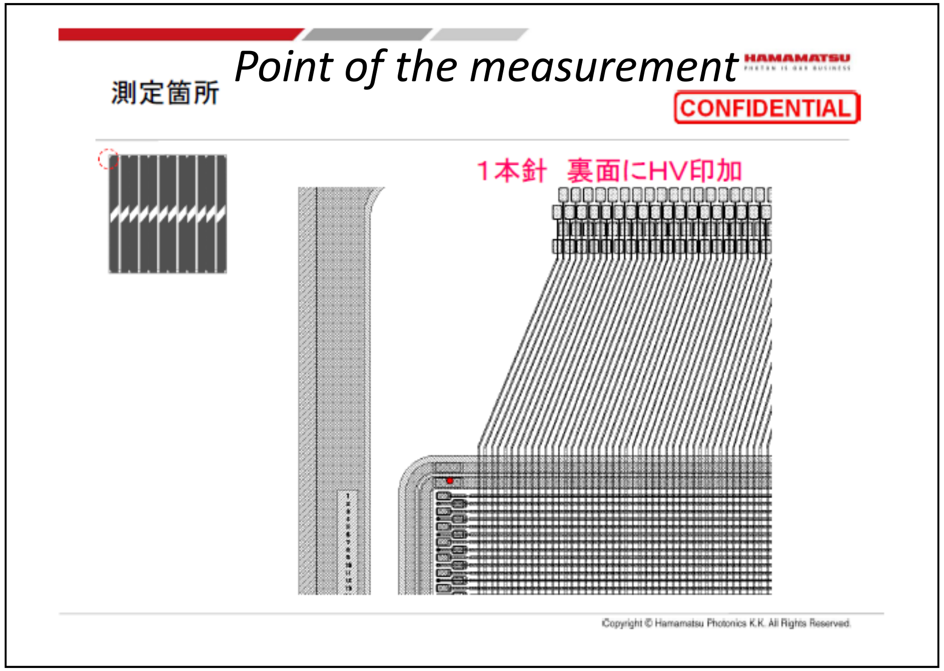


- S2 sensor prototype made by HPK
  - 96 mm x 92.16mm active area
  - 320 um thick
  - AC coupled
  - 6x128x24 mini-trips (60μm x 8mm)
  - 128x24 read-out channels
- All 5 sensors ordered are now at RIKEN
- For all of 5 delivered sensors were tested at HPK
  - No NG channels or strip
  - Vfd = 50 V
  - Vbreakdown > 250V (>500V for two)

Id, Ct measurement



Measure the capacitance when the reserse voltage is applied to the entire chip



Single needle.
HV is applied on backside

Result of the inspection by HPK

Certificate of inspection

日本原子力研究開発機構　御中				1／2 ２０１５年０２月２３日		
検　査　成　績　書				浜松ホトニクス株式会社 固体事業部　第３０部門		
型　名	S10938-3981(X)	判定		責任者		検査員
数　量	2					
備　考						
■受注品　、　□サンプル品　、　□その他				□分納　、　■完納		

以下の２個を納入します
No.1-2

下記の検査結果については、２ページ目以降をご参照ください。

I-V カーブ (0-200V)
全空乏化電圧　Vfd
NG チャンネルリスト(Coupling short、AL open、AL short、Implant open、Implant short、Poly-Si short、Poly-Si open、Bad isolation)

ポリシリコン抵抗モニターパターン測定値

Max.　18.9 MΩ，Min.　15.6 MΩ，Avg.　16.4 MΩ

検査日	２０１５年	２月	０５日	25℃±5℃

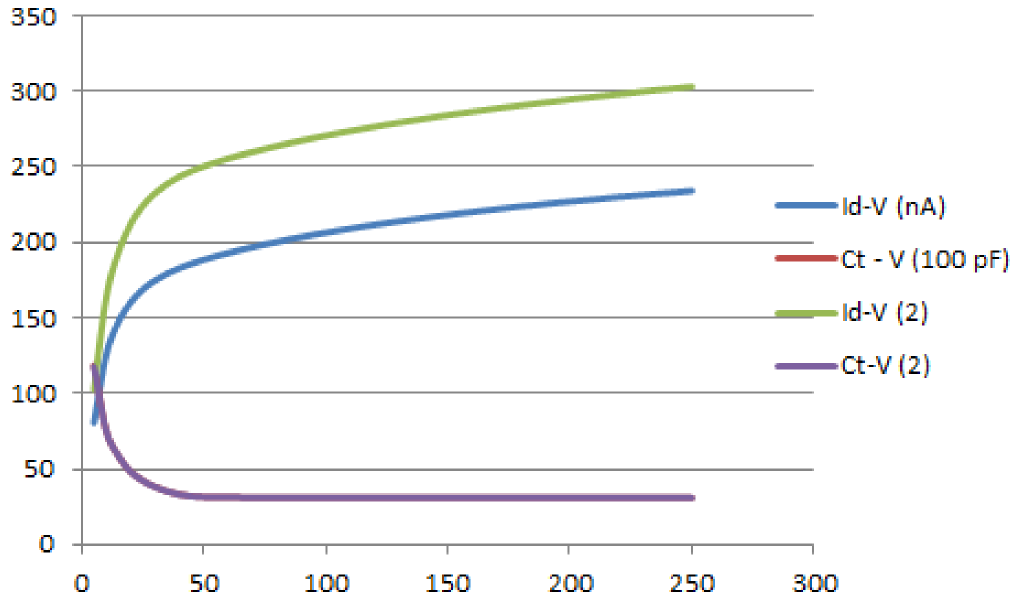
様式K３０－２０１７

浜松ホトニクス株式会社

- All 5 sensor chips are delivered with the certificate of inspection
- I-V/C-V curve
- Vfd (full depletion voltage)
  - Vfd ~ 50 V for all 5
- Breakdown voltage
  - 525 and 650 V for the first 2 sensors
  - > 250V for the other 3 sensors
- List of NG channels
  - 0 NG strips
  - 0 NG channels
- Polysilicon resistance
  - Average 16.4Mohm
  - (spec 5M to 15M)
  - Slightly out of range, but not an issue.

I-V, C-V data for the first 2 sensors

Serial. No. / Vr	1		2	
	Id [nA]	Ct [pF]	Id [nA]	Ct [pF]
5 V	80.4	11878.3	102.7	11774.7
10 V	125.4	7549.6	163.2	7530.3
15 V	147.0	5871.2	192.9	5878.8
20 V	160.2	4822.0	211.9	4813.4
25 V	168.8	4226.2	224.3	4216.4
30 V	174.7	3819.8	232.5	3810.9
35 V	179.3	3523.5	238.7	3515.9
40 V	182.9	3316.4	243.5	3310.3
45 V	185.9	3195.9	247.2	3191.6
50 V	188.5	3147.9	250.3	3143.8
55 V	190.8	3127.2	253.0	3122.5
60 V	192.9	3115.9	255.5	3111.6
65 V	195.0	3107.7	257.8	3103.8
70 V	196.9	3103.0	259.9	3099.7
75 V	198.7	3099.6	261.9	3096.5
80 V	200.3	3097.5	263.8	3093.6
85 V	202.0	3095.4	265.7	3091.2
90 V	203.5	3093.7	267.4	3088.8
95 V	205.0	3091.8	269.1	3088.5
100 V	206.4	3090.7	270.7	3086.9
105 V	207.8	3089.7	272.3	3085.6
110 V	209.1	3088.1	273.7	3084.6
115 V	210.4	3087.1	275.2	3083.9
120 V	211.6	3086.9	276.6	3082.7
125 V	212.8	3085.5	278.0	3081.9
130 V	214.0	3084.9	279.3	3080.8
135 V	215.0	3084.3	280.5	3080.8
140 V	216.1	3083.3	281.8	3079.7
145 V	217.2	3082.8	283.0	3079.5
150 V	218.2	3082.4	284.2	3078.8
155 V	219.2	3082.2	285.4	3078.4
160 V	220.1	3081.4	286.5	3077.8
165 V	221.1	3081.0	287.5	3076.8
170 V	222.0	3080.3	288.7	3077.1
175 V	222.9	3080.1	289.7	3076.3
180 V	223.8	3079.9	290.7	3076.3
185 V	224.6	3079.3	291.7	3075.6
190 V	225.5	3078.7	292.7	3075.2
195 V	226.3	3079.4	293.6	3074.8
200 V	227.0	3078.4	294.6	3073.8
205 V	227.8	3078.3	295.5	3074.1
210 V	228.5	3077.9	296.4	3073.8
215 V	229.3	3077.1	297.3	3073.5
220 V	230.0	3077.0	298.1	3072.6
225 V	230.7	3076.8	298.9	3073.0
230 V	231.4	3076.5	299.9	3072.5
235 V	232.1	3076.4	300.7	3072.1
240 V	232.8	3075.9	301.5	3072.1
245 V	233.4	3075.9	302.3	3071.4
250 V	234.1	3075.4	303.1	3071.6
Vfd [V]	50		50	
NG Strip	Nothing		Nothing	



- Vfd: 50V
- No NG channels
- Breakdown voltage
  - ~ 525 V for sensor 1
  - ~ 650 V for sensor 2

JSPS grant proposal

- I submitted a large KAKENHI grant proposal for to JSPS in last October
  - JSPS is the main funding agency in Japan. Its function is similar to NSF in the US
- Grant Title: sPHENIX experiment: study of quark gluon plasma by using jet probes

  PI: YA Co-PI: ShinIchi Esumi and Shigaki Kenta
- The grant asked for total of 5 oku-yen (~$5M) over 5 years from JFY2015 to JFY2019. The end date of the grant period is March 2020.
  - In the JSPS grant system, we receive the full amount of the allocated fund. Overhead will be provided separately.
- The grant passed the first level selection process and we went to hearing on March 26. About 20% of applicants can go to hearing. Half of them are approved.
- On April 30, I heard that my grant was not approved. I will try again next year.

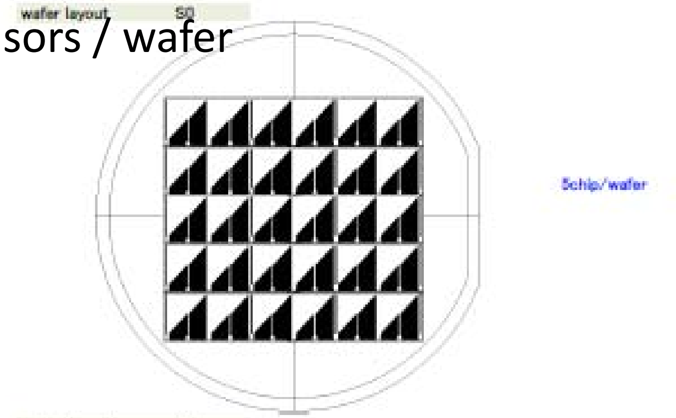
Next step for silicon tracker

- Although I didn’t get the JSPS grant, I have other fund to continue the work in this JFY.
- I think the fund is sufficient to do several things in this JFY if there is enough manpower, in particular engineering resource
  - 1 or 2 rounds of sensor prototyping
  - Develop the first prototype of the ROC (or read-out hybrid)
  - Develop the first Silicon module
  - Some preliminary mechanical design work

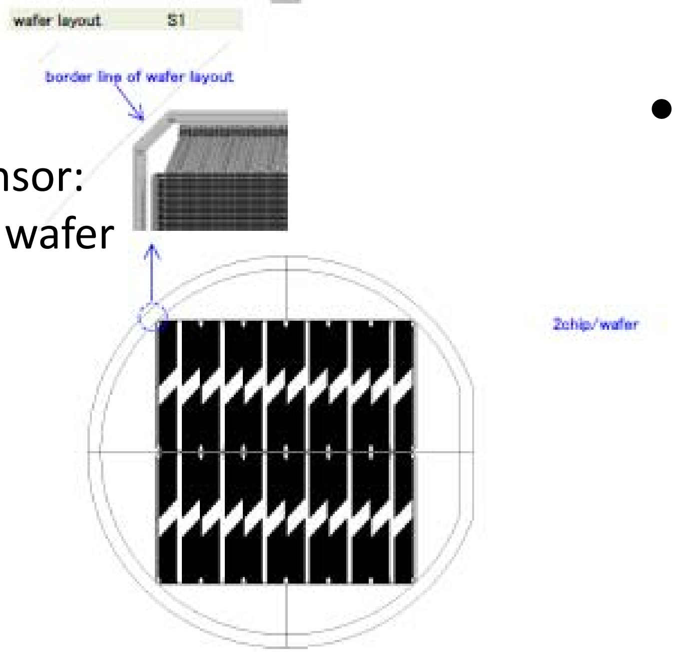
sensor R&D

From HPK. April 15

S0 sensor:
5 sensors / wafer



S1 sensor:
2 in 1 wafer



- I asked pre-design of S0 and S1 sensors

  S0: ~1.6cm x 10cm

  S1: ~5cm x 10cm

  to see how many sensors can be made in one wafer
- We are also considering to make a new S2 prototype for Fpix chip
  - The S2 prototype we just made is for SVX4 pad pattern
  - Power consumption of Fpix is only 20-30% of SVX4

A Design issue

- The momentum resolution, in particular at lower pT, is limited by the multiple scattering . Minimizing the radiation length of this layer is one of most important issue
- The majority of the radiation length is from “stave” which provide mechanical support and cooling
- To achieve small radiation length, air cooling of S1 layer is desirable
- The current design assume SVX4 readout, since PHENIX had so far used this chip for two projects (stripixel and MPC-EX). A drawback of SVX4 is that it generates a relatively large amount of heat (~0.4 watt per chip = 128ch). It is unclear if air cooling is possible.
- FPIX chip used FVTX generates only 20 % of heat of SVX4.

  FPIX 64mW/chip SVX4 300mW/chip (both 128ch)
- We have done no engineering on this issue. We need thermal and mechancial design of stave to evaluate the feasibility of air cooling of either SVX4 or FPIX (or other) solution.

Air cooling calculation (by YA)

$W = \gamma\, C\, Q\, \Delta T$

W: removed heat (watt=J/s)
γ : density of the gas (kg/m^3)
C : specific heat of the gas (J/kg K)
Q: flow rate (m^3/s)
ΔT: increase of the gas temperature (K)
for air at 1atm, γC = 1150 J/m^{3}K = 1.15J/liter K (K: Kelvin)

For S1ab layer, we have

24 SVX4/module x 8 module/ladder x 0.3w/SVX4 ~58 w/ladder

→ Q ΔT ~ 50 K liter/s

For ΔT = 10 K (10 deg C), Q=5 liter/s = 300 l/min

If the cooling gas flows in 8cm x 1cm cross section, flow speed is about 6.25 m/s or 14 miles/h

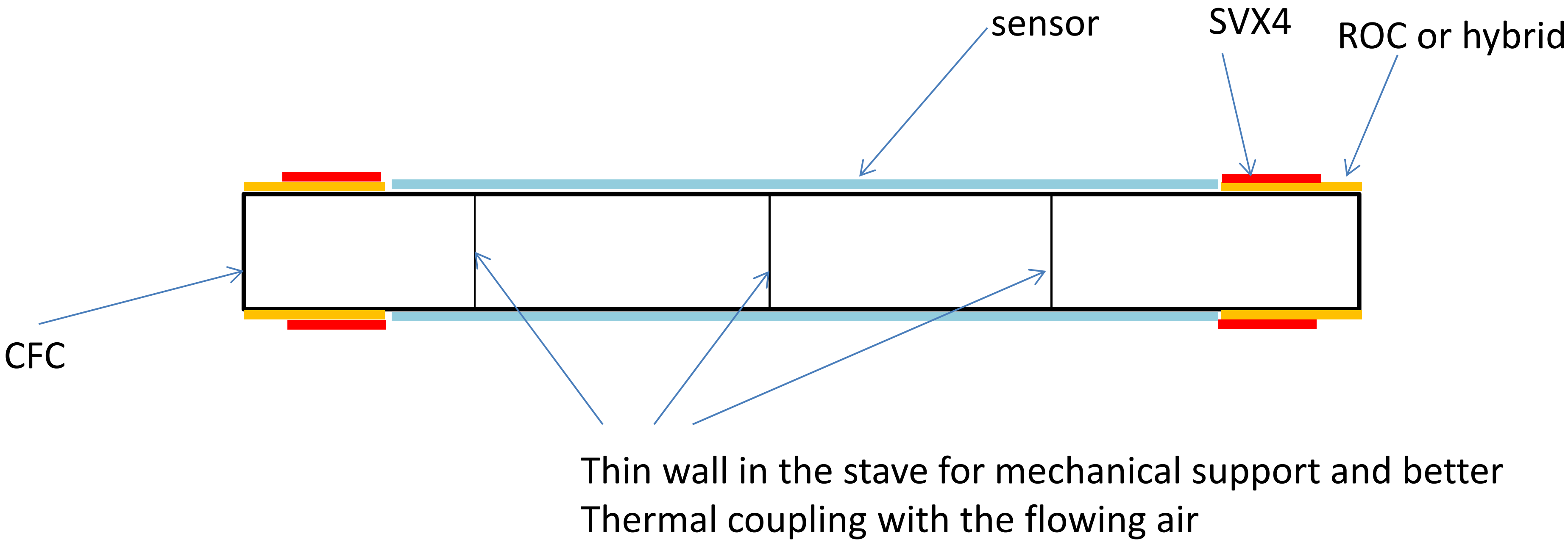
(8cm = 5cm sensor width + 2x1.5cm (Roc width)

I think this is feasible to do. But need actual engineering (stability, thermal stress, etc)

If FPIX is used for read out, we have 20 FPIX per sensor. (Explain later)

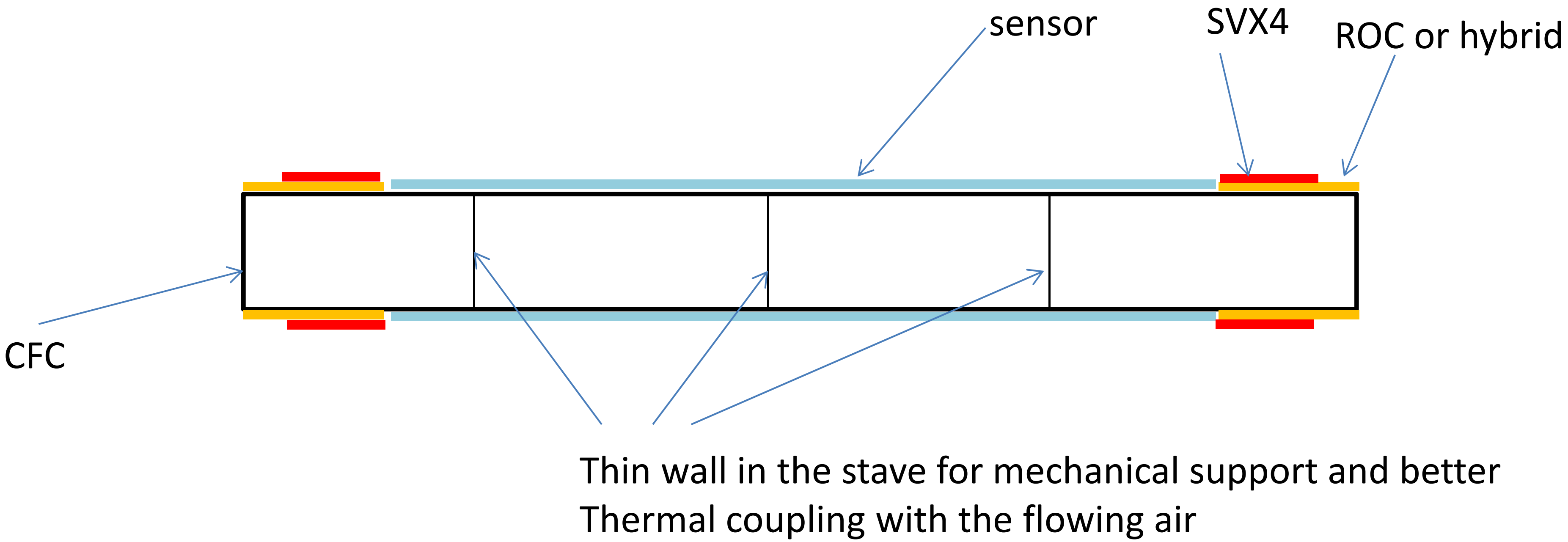
→ W i~10 w/ladder and Q ΔT ~ 8 K liter/s

Stave for air cooling scenario



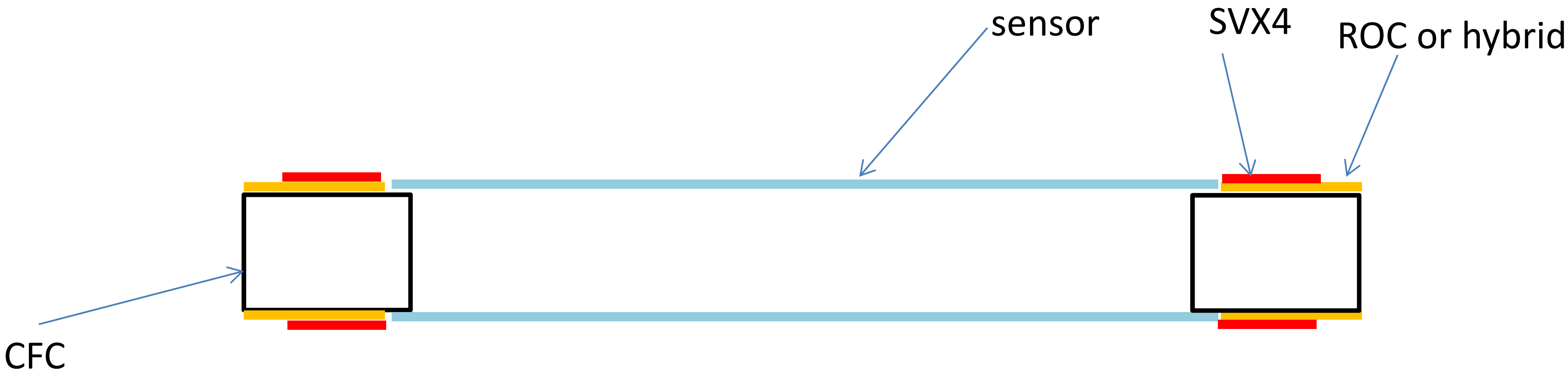
- The gas flows in the stave made of CFC.
- The stave is wider than the sensor (5cm wide) to support ROC. SVX4 is on the ROC and it is the heat source. For 1.5cm wide ROC and 1cm thick stave, there is 8cm^2 of space to flow the gas
- If the flow direction is opposite in the left and the right half of the stave, the temperature gradient of the sensor along the z direction should become almost zero and sensor temperature is higher than the gas by 1/2ΔT (ΔT: increase of the gas temperature)

Material budget guestimate



- Si sensor   (320um)   0.34%
- Stave: 0.1% if the wall thickness is 250um
  ~ 0.2% per sensor area (50% in “wing” + 50% inside)
- ROC: ~0.2% averaged over the sensor area.
- Total 0.74% for one side. (1 sensor layer)
- For double layer, total is just 1.5%
  – Need engineering to see if this is really possible.

Material budget for FPIX



- Air cooling channel under ROC is probably sufficient to cool the system.
- This will save 0.3% radiation length relative to the previous page.

→1.2% radiation length for double layer

This can further reduce the size of the detector. (R~50cm)

Fpix read-out option

- Start working on this possibility
- Discussion with Hubert, Doug and Itaru
  - Length of Fpix is 9mm. So it is not compatible with the HPK sensor we made. This means if we pursue this option, we need to make a new sensor prototype that matches read-out pad pattern of Fpix
  - The new sensor should have 12x10 cells instead of 12x12
    - The mini-strip length in the cell is 9.6mm instread of 8mm. This allows 0.6mm spacing between two Fpix chips. (FVTX HDI has 0.47mm gap between Fpix.)
    - A ROC has 10 Fpix chip.
  - The small HDI of FVTX has 10 Fpix chip. This means that a ROC can be made so that it is compatible with the existing FVTX test bench.
    - Same electronical schematics as the small wedge HDI to read 10 Fpix
    - Same Hirose connector for output bus to connect with FVTX test bench
- Using Fpix for read-out is very attractive
  - Much smaller power consumption (20% of SVX4)
  - The experience and resource of FVTX

Plan (still in making)

- Two prong approach (SVX4 and FPIX)
- SVX4:
  - Send the 5 HPK sensor to BNL
  - Rachid test them with the test bench at Physics
  - Explore the possibility how to read out the sensor with SVX4.
    - The sensor is made for SVX4)
    - SVX4 read-out is good to evaluate the sensor (8bit ADC → can measure MIP S/B ratio)
- Fpix
  - Plan is still in making
  - A probably scenario:
    - Make a new sensor (12x10) for Fpix at HPK (~3-4 months)
    - Develop Fpix read-out hybrid for the new sensor in paralell. The read out hybrid should be compatible with the existing FVTX test bench
    - When both are made, combine them to make a silicon module and test it with Fvtx test bench

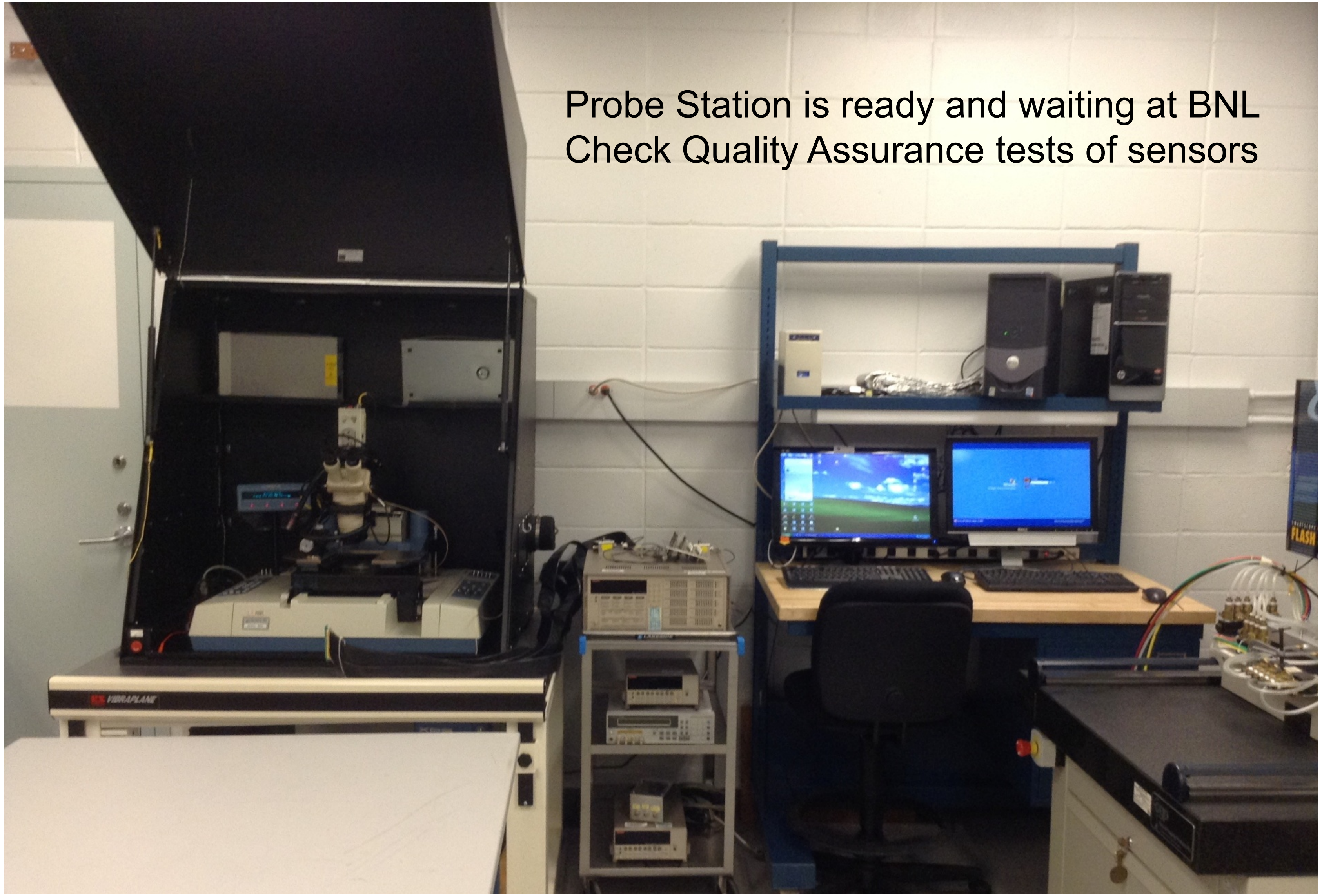
Some additional thought on design

- The current configuration (2 layer in S0(inner), 2 layer in S1(middle), and 1 layer in S2(outer)) is minimum to limit cost
  - Not robust if some of the layer has dead channel
- It is possible to increase the # of layers in S0 with a very small cost impact. For air cooling, the increase of the radiation length is also small (less than 1% per layer)
- So far we consider that the sensor is read-out in both side. This could have geometrical problem for small radius. One side read-out with “barrel” configuration could be a better solution. I will consider this as well.

BNL: Rachid and Rob Pisani

Slide by Rachid

- Probe station at BNL is ready
- Rachid is waiting to get the 5 silicon sensors from RIKEN
  → check sensors specification and Quality Assurance (QA): to prepare sensors to assemble prototype modules: goal is S/N



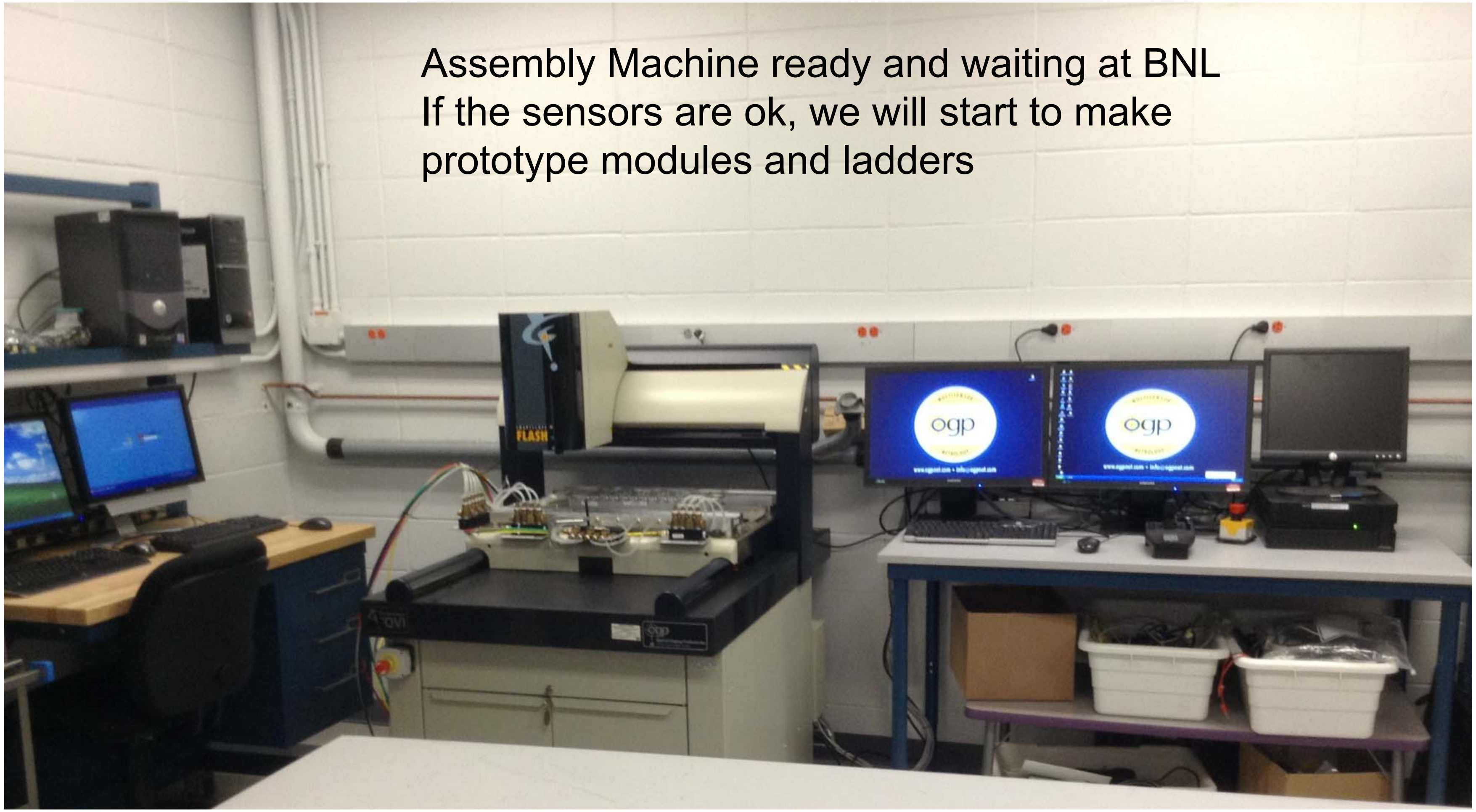
Probe Station is ready and waiting at BNL
Check Quality Assurance tests of sensors

BNL: Rachid and Rob Pisani

Slide by Rachid

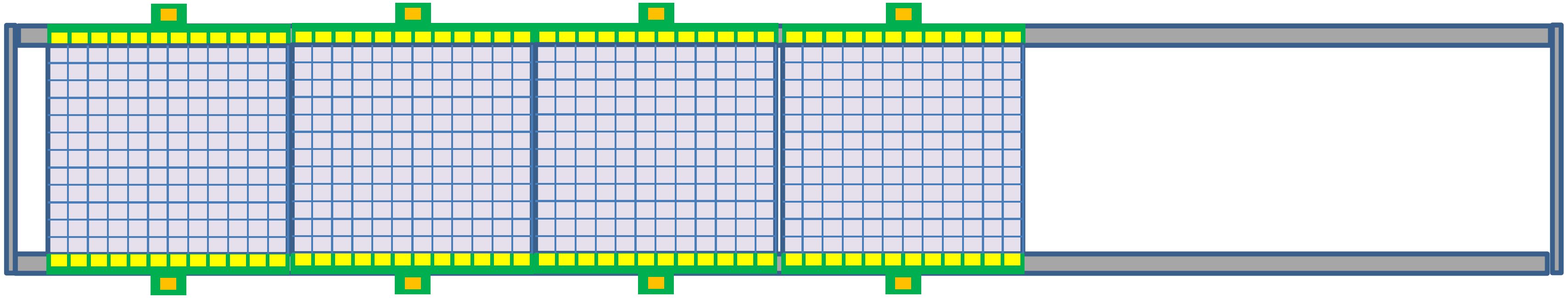
- Assembly machine at BNL ready
- When sensors are accepted by QA, the module concept is define, we can start to make silicon modules/ladder prototypes

→ We can use 90Sr source to determine S/N (crucial)



BNL: Rachid

Slide by Rachid



- May 11, Veljko Radeka and Rachid had a meeting to discuss SVX4 power dissipation and possibility to replace SVX4 chip with a chip with low power dissipation
  → expert on chips readout at the instru. Div. will be back next week

- Another meeting in next few weeks with Gregory Deptuch and Rachid (originally from Strasbourg, FNAL) expert on readout chips.

→ the goals:

- to have prototype readout/silicon modules as close as possible to the final configuration

- remove liquid cooling (replace by air cooling) if possible by selecting chips with low power dissipation (working on it)

Summary

- sPHENIX silicon tracker concept
  - “simple” single sided AC coupled sensor
  - Use technology that we already have experience
  - Minimize the R&D cost
- First prototype sensor delivered.
  - Very good result, according to the test by HPK
- Making a plan to the next stage
  - Two prong approach with SVX4 and FPIX readout
  - Availability of the technical and engineering resource is more of the issue
  - I want to finalize the plan soon